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a transistor provided on said planarized surface of said resinous layer, said transistor comprising:

a semiconductor layer [comprising silicon provided over said resinous layer] comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

*APB*

5. (Amended) A semiconductor device comprising:

a [filmy] resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said [filmy] resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of [comprising a semiconductor layer comprising silicon on] said resinous layer;

an interlayer dielectric layer comprising a resinous material provided over said [semiconductor layer] thin-film transistor; and

an indium tin oxide layer provided on said interlayer dielectric layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

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a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and  
wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

Please add new claims 11-16 as follows:

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-11. A semiconductor device comprising:  
a resinous substrate having an uneven surface;  
a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and  
a transistor provided on said planarized surface of said resinous layer, said transistor comprising:  
a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;  
a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,  
wherein said semiconductor layer comprises microcrystalline silicon.

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12. A semiconductor device comprising:  
a resinous substrate having an uneven surface;  
a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and  
a transistor provided on said planarized surface of said resinous layer, said transistor comprising:  
a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;  
a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,  
wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

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13. The device of claim 11 wherein said substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

14. The device of claim 12 wherein said substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

15. The device of claim 11 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, 2-ethylhexyl ester of acrylic acid.

16. The device of claim 12 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, 2-ethylhexyl ester of acrylic acid.

#### REMARKS

Claims 1-10 were pending in this application. Claims 9 and 10 have been canceled, claims 1 and 5 have been amended and new claims 11-16 have been added hereby. Accordingly, claims 1-8 and 11-16 are now pending in this application and are believed to be in condition for allowance for the reasons stated below.

Paragraph 1 of the Office Action required that a proposed drawing correction be submitted to correct "the noted defect." However, except for the objections summarized on form PTO-948, Applicants are not aware of any issues related to the drawings. Accordingly, Applicants intend to file formal drawings upon receipt of a Notice of Allowance in this case.

Paragraph 3 of the Office Action rejected claims 1, 3 and 9 under 35 USC §102(e) over Tsumura et al., paragraph 7 of the Office Action rejected claims 2, 4-6, 7-8 and 10 under 35 USC §103(a) over Tsumura et al. and Wakai et al., and paragraph 11 of the Office Action rejected